53502

LATCHING SOLID STATE POWER CONTROLLER

Features:

- SPST, Normally Open
- I^2t Circuit Protection
- 1A, 2A Pin Configurable Operating Current
- Switch Status Output
- Power FET Output with Low On-State Resistance
- Operating Temperature Cycle -55°C to +125°C
- Available Military Environmental Screening

Applications:

- 28V bus applications
- Aircraft Power Distribution
- Military/High Reliability Systems
- Satellite/Space Systems

DESCRIPTION

The 53502 Solid State Power Controller is lightweight, resistant to damage from shock and vibration, and immune to contact-related problems (contamination, arcing) associated with mechanical equivalents. Control and Status is user powered by a 4.5 to 5.5V input. The Output is isolated from Control / Status, Bias and Case. The Output is configurable for 1A or 2A High or Low side Load switching. An isolated Bias power supply is provided to operate the Output circuits and may be powered from the load bus or a separate power source. The control input is CMOS compatible and operates from a supply of 4.5 to 5.5VDC (See Figure 1).

The Latching feature allows the Output state to remain as commanded in the event of loss of 5V Logic power.

Transformer coupling between the input, output and Bias power stages provides isolation up to 500 V RMS. The Power MOSFET output minimizes output voltage drop.

Integral short-circuit protection, I^2t trip and Output Status is provided. The sensed output current circuit responds to over-current with an I^2t trip curve by opening the output. An open-collector output status indicates the switch state. The output will remain blocked indefinitely until the short is removed and the unit reset. This feature prevents damage to the controller and averts further system failures that may be caused by the short circuit. Output Status is On (High) when the output is switched On and is Off (Low) whenever the output is commanded off or tripped. Resetting the unit is accomplished by cycling the input control.

ABSOLUTE MAXIMUM RATINGS

Isolation voltage[1]	500 V RMS
Continuous operating output voltage[2]	100 VDC
Transient output voltage	100 VDC
Load Current (Self Limiting)	18A / Self Limiting
Input supply voltage, V_{DD}	4.5 to 5.5 VDC
Operating temperature	-55ºC to +125ºC Case
Storage temperature	-65ºC to +125ºC

Notes:
[1] 60 Hz sine wave
[2] Reversing polarity on the output may cause permanent damage

ELECTRICAL CHARACTERISTICS

T_A = -55°C to 125° C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics CMOS Configurations (Figure 1)					
$V_{DD\ Input}$		4.5		5.5	VDC
Control Input current	5 VDC Input			500	µA
Control voltage range		-0.5		5.5	VDC
Turn-on voltage	At V_{DD} = 5.0V		2.8	3.4	VDC
Turn-off voltage	At V_{DD} = 5.0V	0.5	2.0		VDC
Dielectric strength (Control / Status to Output to Bias to Case)	60 Hz	500			V RMS
Bias Characteristics					
Bias current I_{Bias}	Note 5		5	10	mA
Bias supply range, V_{Bias}	Note 6		28	50	VDC
Output Characteristics					
Output current, sustaining:					
Continuous blocking voltage	Note 7			100 / 50	VDC
On-state resistance, R_{ds} (1A Configuration)	25ºC Case		.1Ω	.13Ω	Ohms
On-state resistance, R_{ds} (2A Configuration)	25ºC Case		.075Ω	.085Ω	Ohms
Turn-on time @ 25ºC case	Figure 2		0.8	2.0	mS
Turn-off time @ 25ºC case	Figure 2		0.5	1.0	mS
Off-state leakage	At Rated Voltage		40	100	µA
Output Capacitance				700	pF
Load Start current	25ºC	6/12	7.5/15	9/18	A
Short-circuit peak				100	A
Trip Reset Time	Remove short / overload & Cycle input	50			mS
Status Output Specification					
Status Supply Voltage (open Collector)		5.0		32	VDC
Status off leakage current	VS = 30 VDC			100	µADC
Status off leakage current	VS = 15 VDC			4	µADC
Status on voltage	I_{STATUS} = 5 MA			0.4	VDC
High-To-Low Transition Time	I_{STATUS} = 5 MA		20	50	µS
Junction temperature				150	ºC
Thermal resistance θ_{JA} θ_{JC}				30 5	ºC/W ºC/W

Application Notes:
1. Maximum input switching frequency not to exceed 10 Hz under normal conditions, or .5 Hz if output is shorted.
2. Input transitions should be <1 ms and duration and input source should be “bounce-less contact” type.
3. Inductive loads must be snubbed or clamped.
4. Peak current that may flow when output is shorted.
5. Current from the Bus input.
6. 50V Maximum for Bias Pins 10 to 5.
7. 100V Maximum for output Pins 9 to Pins 6, 7 and/or 8.

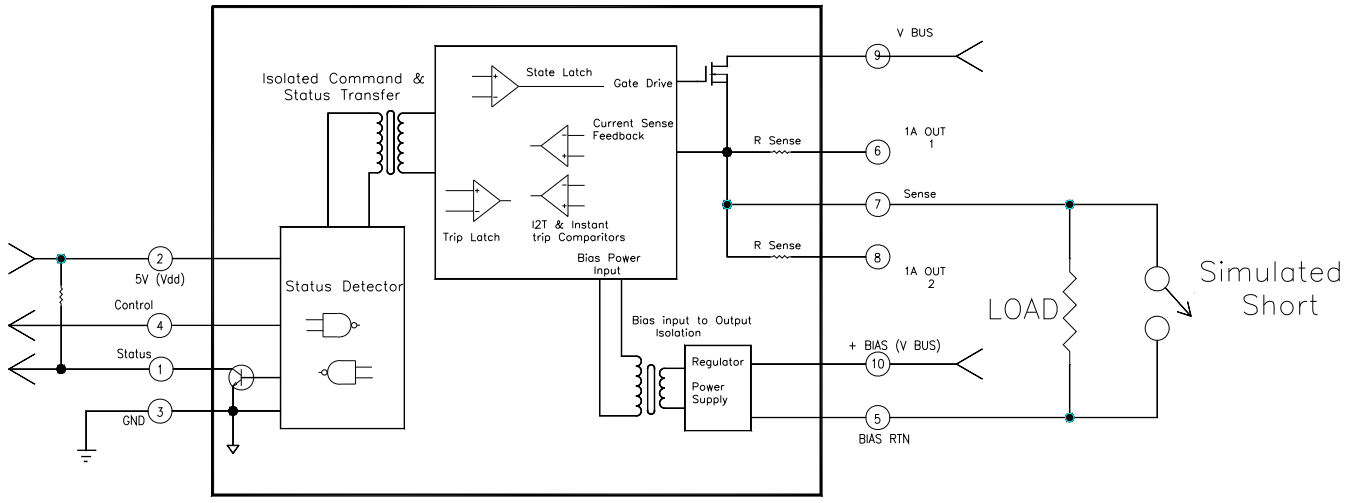


FIGURE 1, Connection Diagram

Connect Pins 6 to 7 or Pins 7 to 8 for 1A Output

Connect Pins 6 to 7 to 8 for 2A Output

See Appendix A for operational description

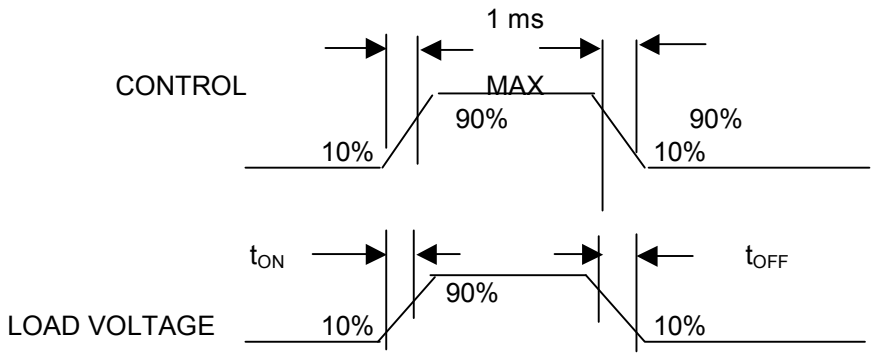


Figure 2 Switching Characteristics

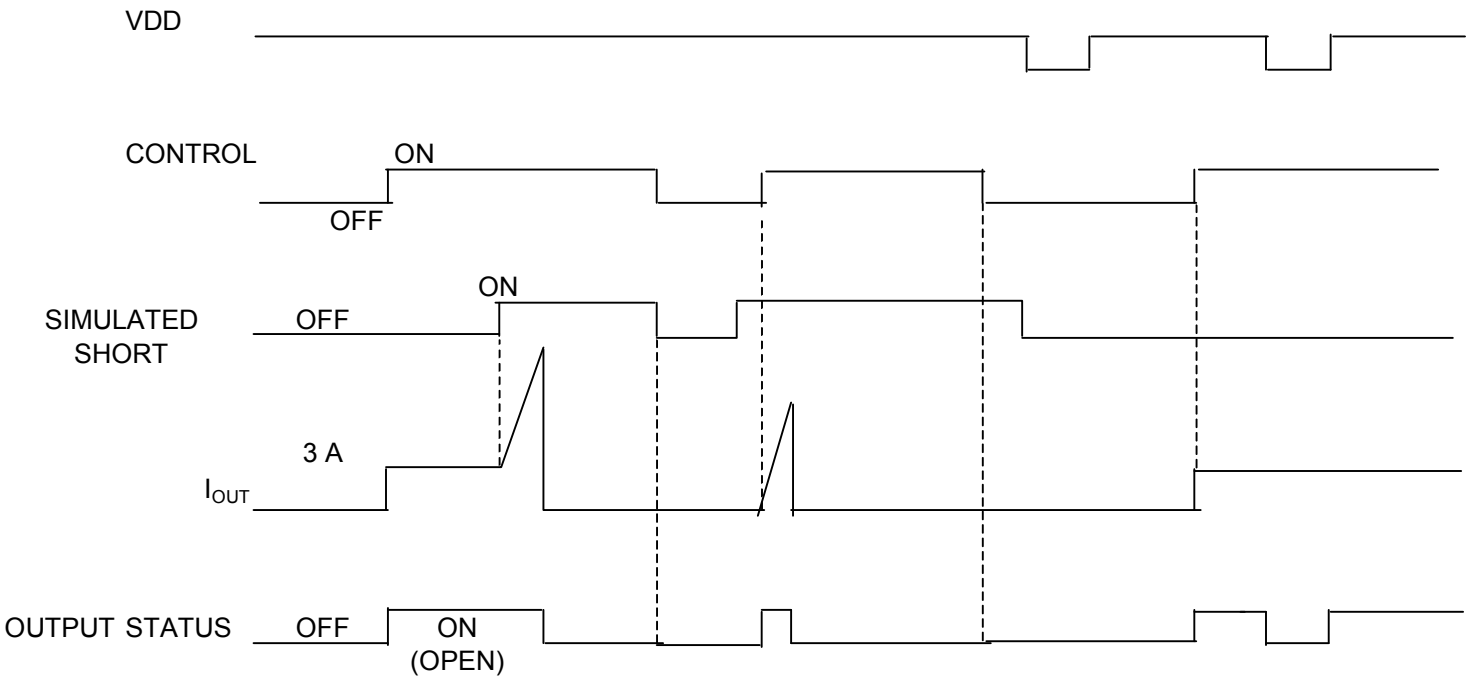


Figure 3 - TIMING DIAGRAM

Notes:

Note 1: A turn-off into a short produces an increase in current to the initial I^2T must trip value.

Note 2: Shorted while On from any On operating condition can have a μs surge current of as much as 100A.

Note 3: Loss of and re-application of Bus power will result in a re-start (output open & Output Status low.)

Note 4: Output Status signal assumes a pull-up voltage is always present to produce a “1” when status is open.

Note 5. Latching feature on 250, 400, and 500V versions is dependant upon uninterrupted Bias Power.

Truth Table – Power Sequencing: Figure 4

Bus Voltage	0	On	0			On	On
V_{DD}	0	0	On				
Control	X	X	X	0		X	X
I Out	Open	Open	Open	Open		0	1
Output Status	Open “1”	Open “1”	0	0			Open “1”
Short	X	X	X	Off	Off	Off	Off
		(Note 1)	(Note 1,2)	(Note 3)	(Note 3,4)	(Note 5)	(Note 5)

Truth Table – Short circuit and Status: Figure 5

	Turn on into Short Sequence						Short while on Sequence			
Control	0	1	1	0	1	1	1	1	0	1
I out	Off	Off	Off	Off	On	On	Off	Off	Off	On
Output Status	0	0	0	0	Open “1”	Open “1”	0	0	0	Open “1”
Shorted Output	Shorted	Shorted	X	Off	Off	Off	On	X	X	Off

Note 1: Unit Powers up in the Off condition with application of either Bus or V_{DD}.

Note 2: Output Status reports only when V_{DD} is present.

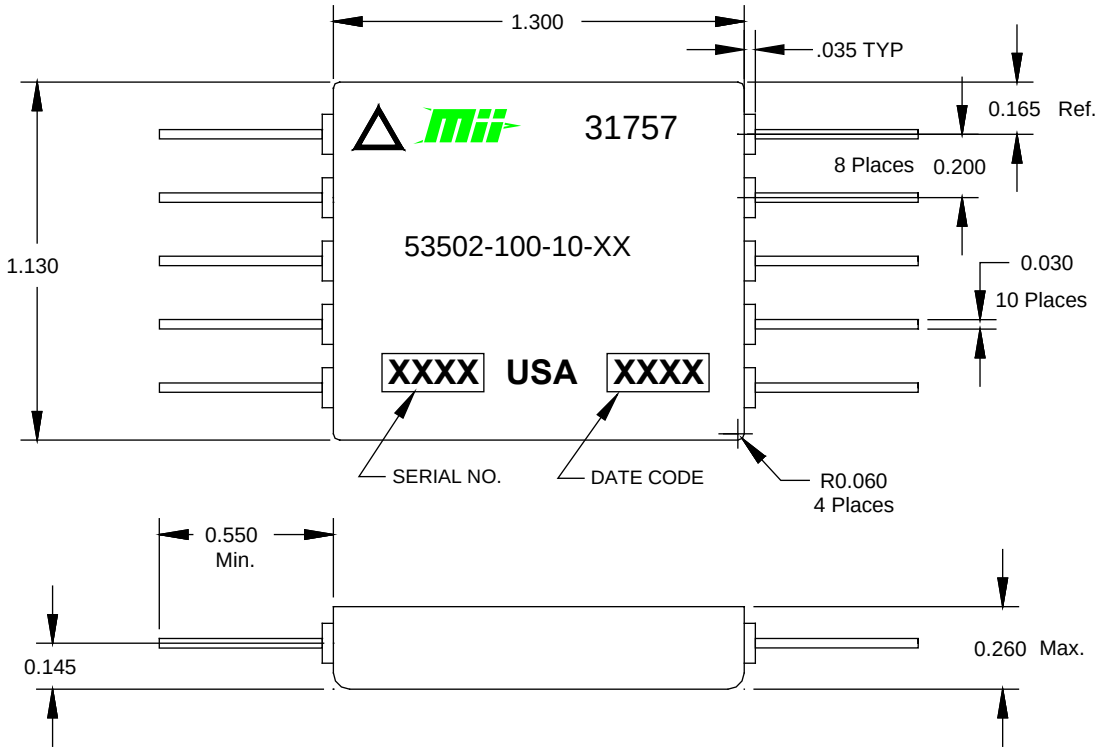
Note 3: Control “0” Off must be invoked upon simultaneous applications of 5V and Bus Power for an unambiguous output and fault status.

Note 4: An Off Control to On Control transition is required to first turn the Unit On.

Note 5: Loss of V_{DD} will not change output state.

Note 6: Truth Table-Power sequencing: Output Status open collector pull-up resistor is assigned a separate and always present voltage, producing a “1” when “Open”.

Package Dimensions
Figure 6



IN	V CONNECTION	
1	OUTPUT STATUS	
2	V_{DD}	
3	CONTROL RETURN	
4	CONTROL	
5	BIAS RETURN (- BUS)	
6	OUT (1A)	
7	OUT SENSE	
8	OUT (1A)	
9	+ BUS	
10	BIAS (+ BUS)	

Notes:
1. For 1A output, connect Pins 6 and 7 or Pins 7 and 8; for 2A output connect Pins 6, 7 and 8.
2. Bias power input at Pins 10 and 5 may be connected to the BUS power or a separate power source.

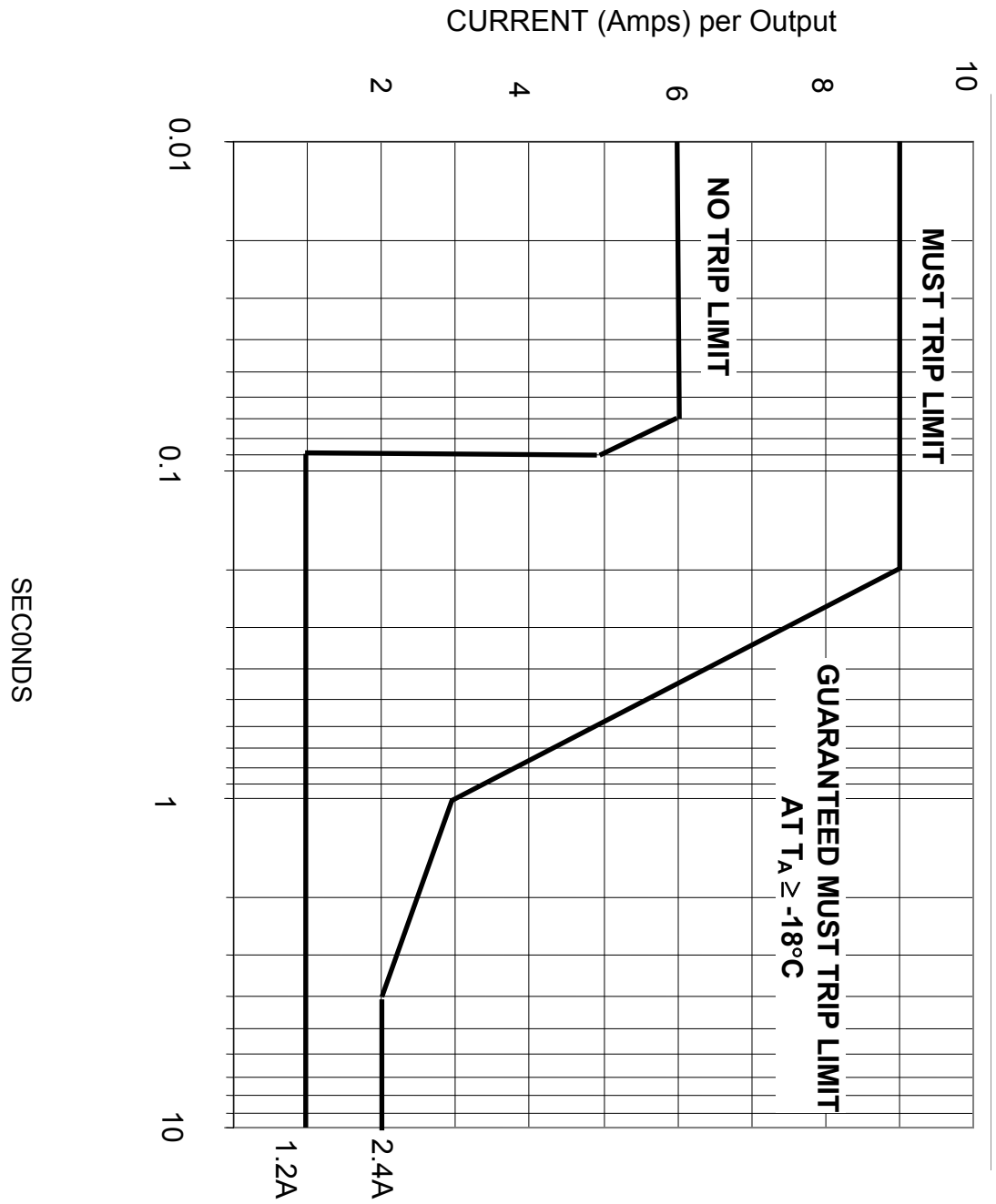
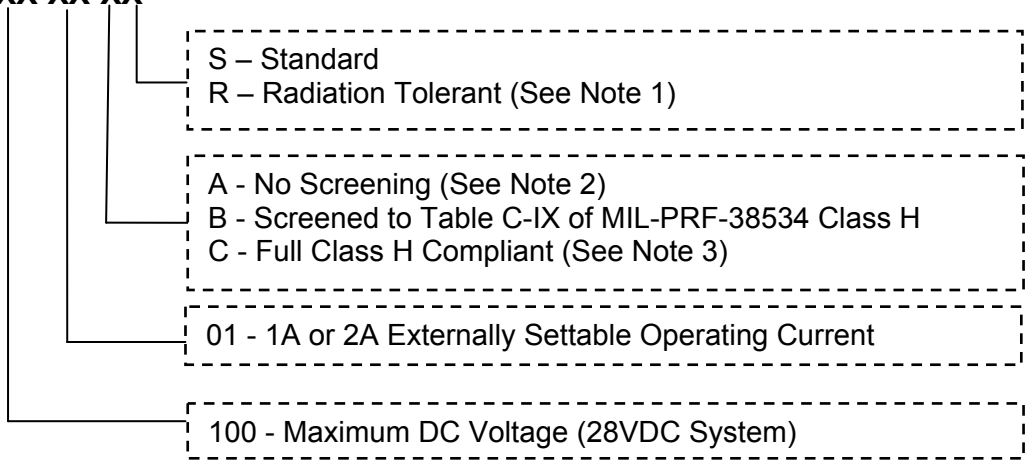


Figure 7

Notes:
1) Initial current limits (NO TRIP and MUST TRIP) will be 6 and 9A for each of the 1A outputs.
2) 1A Output (Case pins 6 and 7 connected together). Output current per graph.
3) 2A Output (Case pins 6, 7 and 8 connected together). Output current two times values of graph.

Ordering Information:

MPC-53502-XXX-XX-XX



Notes:

1. The device contains radiation hardened components and/or other features that provide a level of radiation tolerance. Micropac does not guarantee any level of radiation hardness. Specific lot testing is required to determine the level of radiation hardness. Micropac does not offer this device as compliant to Appendix G (RHA Requirements) of MIL-PRF-38534.

2. Devices are electrically tested at -55°C, +25°C and +125°C with no environmental screening or qualification.

3. Fully compliant Class H devices will require Element Evaluation and QCI.

4. Contact factory for custom voltage, current and feature combination.

Appendix A: Operational Description

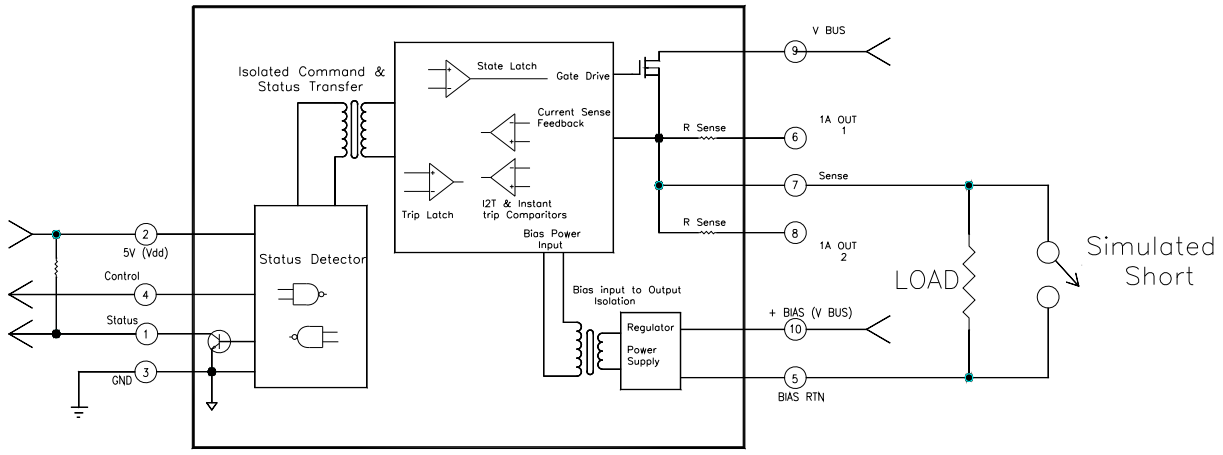


FIGURE 1, Connection Diagram

Connect Pins 6 to 7 or Pins 7 to 8 for 1A Output
Connect Pins 6 to 7 to 8 for 2A Output

The 53502 functions include:

1. Logic connected components
2. Bus connected MOSFET output switch
3. Bus connected control functions
4. Bias regulator and power supply

1. The logic connected components consists of the 5V (4.5 to 5.5V) customer furnished operating power, the Open Collector Status output and detector circuits, the control input and transformer isolation drive circuit. The internal logic is CMOS with compatibility with TTL and NMOS circuits.

2. The Bus connected MOSFET output switch is isolated from all other circuit elements (Logic connected components, Bias inputs and Case). This allows operation as floating switch which may be connected as a High side or Low side switch. Pins 6 and 8 have a dedicated sense resistor for each output and when either is connected to Pin 7 (Sense) a feedback voltage is made available to the Bus connected control functions to allow a 1A output. Pins 6 or 8 tied to pin 7 allows an output of 1A and connecting Pins 6, 7 and 8 allows an output of 2A per the I^2t curve of Figure 7.

3. Bus connected control functions are referenced to the Output Sense Pin 7 and isolated from Logic connections, Bias inputs and Case. The Control input transformer secondary operates the State Latch and resets the Trip latch. On power up, the Trip latch is designed to initialize in the tripped state preventing an accidental ON condition. A Control Low (OFF) ensures the State latch and gate drive is OFF and resets the Trip Latch. The following Control ON and all commands following the initial ON provide like output from the output MOSFET. Current sense feedback is monitored for I^2t and over-current. Out of bounds currents are detected and set the Trip latch which in turn shuts the MOSFET gate drive OFF. Also, Status OFF information is fed back across the input transformer and reported through the Status Output.

4. The Bias circuit pre-regulates the 28V Buss input and generates the various isolated voltages and signals for the internal functions.